WHAT IS CLAIMED IS:

1. A mass storage data protection system for use with a mass storage device in a gaming machine, the mass storage data protection system comprising:

a mass storage device command latch;

a timing circuit for timing signals between the mass storage device command latch and the mass storage device;

a comparator between the mass storage device command latch and the timing means; and

a comparator command register in communication with the comparator, the comparator command register including commands that generate a fault within the mass storage data protection system;

wherein when the comparator receives a command from the mass storage device command latch corresponding to a command within the comparator command register, a fault is generated within the mass storage command latch.

2. A mass storage data protection system in accordance with claim 1 further comprising a control and status register in communication with the comparator command register and the comparator, the control and status register being configured to at least partially control functioning of the mass storage data protection system.

3. A mass storage data protection system in accordance with claim 1 wherein the timing circuit comprises a synchronizer and a reset generator.

4. A mass storage data protection system in accordance with claim 1 wherein the mass storage device consists of an intelligent drive electronics hard disk drive and the mass storage device command latch consists of an intelligent drive electronics command latch.

5. A mass storage data protection system in accordance with claim 1 wherein the comparator command register comprises a fixed command array and a user command array.

6. A mass storage data protection system for use with an intelligent drive electronics mass storage device in a gaming machine, the mass storage data protection system comprising:

an intelligent drive electronics command latch;

a timing circuit for timing signals between the intelligent drive electronics command latch and the intelligent drive electronics mass storage device, the timing circuit comprising a synchronizer and a reset generator;

a comparator comprising a fixed command array and a user command array, the comparator being located between the intelligent drive electronics command latch and the timing circuit;

a comparator command register in communication with the comparator, the comparator command register including commands that generate a fault within the mass storage data protection system; and

a control and status register in communication with the comparator command register and the comparator, the control and status register being configured to at least partially control functioning of the mass storage data protection system;

wherein when the comparator receives a command from the intelligent drive electronics command latch corresponding to a command within the comparator command register, a fault is generated within the intelligent drive electronics command latch.

7. A gaming machine comprising:

a housing;

at least one user input coupled to the housing;

a display coupled to the housing; and

a control system, the control system comprising:

a mass storage device; and

a mass storage data protection system, the mass storage data protection system comprising:

a mass storage device command latch;

a timing circuit for timing signals between the mass storage device command latch and the mass storage device;

a comparator between the mass storage device command latch and the timing circuit; and

a comparator command register in communication with the comparator, the comparator command register including commands that generate a fault within the mass storage data protection system;

wherein when the comparator receives a command from the mass storage device command latch corresponding to a command within the comparator command register, a fault is generated within the mass storage command latch.

8. A gaming machine in accordance with claim 7 further comprising a control and status register in communication with the comparator command register and the comparator, the control and status register being configured to at least partially control functioning of the mass storage data protection system.

9. A gaming in accordance with claim 7 wherein the timing circuit comprises a synchronizer and a reset generator.

10. A gaming machine in accordance with claim 7 wherein the mass storage device consists of an intelligent drive electronics hard disk drive and the mass storage device command latch consists of an intelligent drive electronics command latch.

11. A gaming machine in accordance with claim 7 wherein the comparator command register comprises a fixed command array and a user command array.

12. A gaming machine comprising:

a housing;

at least one user input coupled to the housing;

a display coupled to the housing; and

a control system, the control system comprising:

an intelligent drive electronics mass storage device; and

a mass storage data protection system, the mass data protection system comprising:

an intelligent drive electronics command latch;

a timing circuit for timing signals between the intelligent drive electronics command latch and the intelligent drive electronics mass storage device, the timing circuit comprising a synchronizer and a reset generator;

a comparator comprising a fixed command array and a user command array, the comparator being located between the intelligent drive electronics command latch and the timing circuit;

a comparator command register in communication with the comparator, the comparator command register including commands that generate a fault within the mass storage data protection system; and

a control and status register in communication with the comparator command register and the comparator, the control and status register being configured to at least partially control functioning of the mass storage data protection system;

wherein when the comparator receives a command from the intelligent drive electronics command latch corresponding to a command within the comparator command register, a fault is generated within the intelligent drive electronics command latch.

13. A gaming machine in accordance with claim 7 wherein the control system further comprises:

a write enable switch in communication with the comparator, the write enable switch being configured to suppress generation of a fault within the mass storage command latch when the write enable switch is closed.

14. A gaming machine in accordance with claim 13, further comprising:

a microprocessor in communication with the mass storage device and the mass storage data protection system; and

gaming machine operating software running on the microprocessor, the gaming machine operating software having at least a gaming mode and a maintenance mode,

wherein the gaming machine operating software is configured to suspend gaming operation when the write enable switch is closed and the gaming machine operating software is in a mode other than the maintenance mode.